CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A system of cascaded devices, comprising:

a first device having a first input for receiving a request signal, a second input for receiving a first reply signal, a first output for outputting said request signal, and a second output for outputting a second reply signal, said second reply signal being generated from operations performed in response to said request signal and from said first reply signal;

at least one buffer coupled to said first device for receiving and outputting at least one of said outputted request signal and said second reply signal, said at least one buffer having an associated latency; and

a second device coupled to receive said outputted request signal and said second reply signal, said at least one buffer being configured to substantially equate a latency of said first device with a latency of said second device.

2. The system of claim 1, further comprising an output bus coupled between said at least one buffer and said second device.

3. The system of claim 1, wherein said at least one buffer is a buffer having a programmable latency.

4. The system of claim 3, wherein buffer latency may be bypassed.

5. The system of claim 1, wherein said at least one buffer buffers said outputted request signal when said second device has a lower latency than said first device.

6. The system of claim 1, wherein said at least one buffer buffers said second reply signal when said second device has a higher latency than said first device.

7. The system of claim 1, wherein said first device and said second device are content addressable memory (CAM) devices.

8. The system of claim 1, further comprising a common output bus coupled to said at least one buffer.

9. The system of claim 1, wherein said at least one buffer is internal to said first device.

10. The system of claim 1, wherein said at least one buffer is internal to said second device.

11. The system of claim 1, wherein said at least one buffer further comprises a first buffer for receiving and outputting said request signal and a second buffer for receiving and outputting said second reply signal.

12. The system of claim 11, wherein said first buffer and said second buffer comprise latencies programmed to equate said latency of said first device with said latency of said second device.

13. A system of cascaded devices, comprising:

a first device having a first input for receiving a request signal from a first source, a second input for receiving a first reply signal from said first

source, a first output for outputting said request signal, and a second output for outputting a second reply signal;

a first programmable buffer coupled to said first device for receiving said outputted request signal; and

a second programmable buffer coupled to said first device for receiving said second reply signal.

14. The system of claim 13, further comprising an output bus coupled between said first and second buffers and a second device.

15. The system of claim 13, wherein said second reply signal is generated from said request signal and said first reply signal.

16. The system of claim 14, wherein said first buffer buffers said outputted request signal when said second device has a lower latency than said first device.

17. The system of claim 14, wherein said second buffer buffers said second reply signal when said second device has a higher latency than said first device.

18. The system of claim 13, wherein said first buffer and said second buffer are internal to said first device.

19. The system of claim 13, wherein said first buffer and said second buffer have programmable depths.

20. The system of claim 19, wherein buffer stages in said first buffer and said second buffer may be bypassed.

21. The system of claim 14, wherein said first device and said second device are content addressable memory (CAM) devices.

22. The system of claim 13, wherein said first and second programmable buffers are part of a same buffer unit.

23. A method for aligning request and reply signals between devices in a system of cascaded devices, said method comprising the steps of:

receiving and outputting a request signal at a first device;

receiving a first reply signal at said first device;

generating a second reply signal at said first device in response to operations performed in response to said request signal and in response to said first reply signal;

outputting said second reply signal;

buffering said request signal if a second device coupled downstream from said first device has a lower latency than said first device; and

buffering said second reply signal if said second device coupled downstream from said first device has a higher latency than said first device.

24. The method of claim 23, wherein said first device and said second device are content addressable memory (CAM) devices.

25. The method of claim 24, wherein said operations performed include a search operation.

26. The method of claim 25, wherein said first device inserts a search hit index into said second reply signal.

27. The method of claim 24, wherein said request signal originates from a host ASIC device.

28. A cascaded system, comprising:

a first device having a first latency;

a second device having a second latency different from said first latency; and

at least one buffer coupled between outputs of said first device and inputs of said second device, said at least one buffer being programmed to transfer signals on the outputs to the inputs by substantially equating said first and said second latencies.

29. The cascaded system of claim 28, wherein said at least one buffer comprises a first buffer and a second buffer.

30. The cascaded system of claim 28 wherein said at least one buffer is internal to said first device.

31. The cascaded system of claim 28 wherein said at least one buffer is internal to said second device.

32. The cascaded system of claim 28, wherein said at least one buffer buffers a request signal outputted from said first device when said second device has a lower latency than said first device.

33. The cascaded system of claim 28, wherein said at least one buffer buffers a reply signal outputted from said first device when said second device has a higher latency than said first device.

34. A processor system, comprising:

a first device having a first input for receiving a request signal, a second input for receiving a first reply signal, a first output for outputting said request signal, and a second output for outputting a second reply signal, said second reply signal being generated from operations performed in response to said request signal and from said first reply signal;

at least one buffer coupled to said first device for receiving and outputting at least one of said outputted request signal and said second reply signal, said at least one buffer having an associated latency; and

a second device coupled to receive said outputted request signal and said second reply signal from said at least one buffer, said at least one buffer being configured to substantially equate a latency of said first device with a latency of said second device.

35. The processor system of claim 34, wherein said first device and said second device are content addressable memory (CAM) devices.

36. The processor system of claim 35, wherein said operations performed include a search operation.

37. The processor system of claim 36, wherein said first device inserts a search hit index into said second reply signal.

38. The processor system of claim 35, wherein said request signal originates from a host ASIC device.

39. A processor system, comprising:

a first device having a first latency;

a second device having a second latency different from said first latency; and

at least one buffer coupled between outputs of said first device and inputs of said second device, said at least one buffer being programmed to transfer signals on the outputs to the inputs by substantially equating said first and said second latencies.

40. The processor of system claim 39, wherein said first device and said second device are content addressable memory (CAM) devices.

41. The processor of system claim 39, wherein said first device receives a request signal and a first reply signal.

42. The processor of system claim 41, wherein said first device generates a second reply signal from operations performed in response to said request signal and from said first reply signal.

43. The processor of system claim 42, wherein said first device and said second device are content addressable memory (CAM) devices.

44. The processor system of claim 43, wherein said operations performed include a search operation.

45. The processor system of claim 44, wherein said first device inserts a search hit index into said second reply signal.

46. The processor system of claim 43, wherein said request signal originates from a host ASIC device.

47. A router, comprising:

a first device having a first latency;

a second device having a second latency different from said first latency; and

at least one buffer coupled between outputs of said first device and inputs of said second device, said at least one buffer being programmed to transfer signals on the outputs to the inputs by substantially equating said first and said second latencies.

48. The router of claim 47, wherein said first device and said second device are content addressable memory (CAM) devices.

49. The router of claim 47, wherein said first device receives a request signal and a first reply signal.

50. The router of claim 49, wherein said first device generates a second reply signal from operations performed in response to said request signal and from said first reply signal.

51. The router of claim 50, wherein said first device and said second device are content addressable memory (CAM) devices.

52. The router of claim 51, wherein said operations performed include a search operation.

53. The router of claim 52, wherein said first device inserts a search hit index into said second reply signal.

54. The router of claim 51, wherein said request signal originates from a host ASIC device.

55. An integrated circuit, comprising:

a first device having a first latency;

a second device having a second latency different from said first latency; and

at least one buffer coupled between outputs of said first device and inputs of said second device, said at least one buffer being programmed to transfer signals on the outputs to the inputs by substantially equating said first and said second latencies.

56. The circuit of claim 55, wherein said first device and said second device are content addressable memory (CAM) devices.

57. The circuit of claim 55, wherein said first device receives a request signal and a first reply signal.

58. The circuit of claim 57, wherein said first device generates a second reply signal from operations performed in response to said request signal and from said first reply signal.

59. The circuit of claim 58, wherein said first device and said second device are content addressable memory (CAM) devices.

60. The circuit of claim 59, wherein said operations performed include a search operation.

61. The circuit of claim 60, wherein said first device inserts a search hit index into said second reply signal.

62. The circuit of claim 59, wherein said request signal originates from a host ASIC device.